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W	AG	Chinnery, D.G. et al., "Achieving 550 MHz in an ASIC Methodology," Department of EECS, University of California at Berkeley, 2001, 6 pages.									
W	АН	Friedman, Eby G., "Clock Distribution Networks in Synchronous Digital Integrated Circuits," Invited Paper, IEEE, Vol. 89, No. 5, May 2001, pp. 665-692.									
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